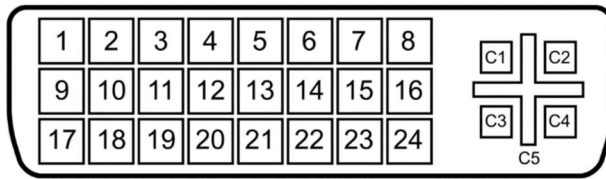


SOPHIA 3

Improved Graphics Television Interface Adapter

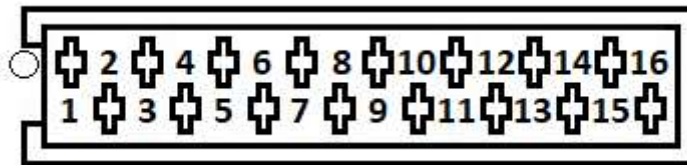
Preliminary

1. DVI-I Output Connector



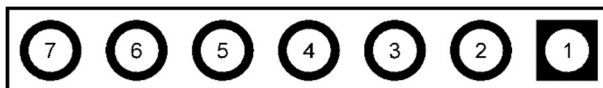
1 – TMDS Data 2 -	11 – TMDS Data 1 Shield	21 – NC
2 – TMDS Data 2 +	12 – NC	22 – TMDS Clock Shield
3 – TMDS Data 2 Shield	13 – NC	23 – TMDS Clock +
4 – NC	14 - +5V 150mA max.	24 – TMDS Clock -
5 – NC	15 – GND	
6 – NC	16 – Hot Plug Detect	C1 – Analog Red/P _R
7 – NC	17 – TMDS Data 0 -	C2 – Analog Green/Y
8 – VSYNC/ RGB Blanking	18 – TMDS Data 0 +	C3 – Analog Blue/P _B
9 – TMDS Data 1 -	19 – TMDS Data 0 Shield	C4 – HSYNC/CSYNC
10 – TMDS Data 1 +	20 – NC	C5 – Analog GND

2. Board-To-Board Connector



1 – Analog Blue	6 – GND	11 – TMDS Data 1 +
2 – Analog VSYNC	7 – GND	12 – TMDS Data 1 -
3 – Analog Green	8 – +5V Out	13 – TMDS Data 0 +
4 – Analog HSYNC/CSYNC	9 – TMDS Data 2 +	14 – TMDS Data 0 -
5 – Analog Red	10 – TMDS Data 2 -	15 – TMDS Clock +
		16 – TMDS Clock -

3. JTAG/UPDI Connector



1 – GND	3 – TDI	5 – TMS	7 – +3.3V
2 – TDO	4 – TCK	6 – UPDI	

4. Registers

DISM0PF	\$D000 (R/W)
DISM1PF	\$D001 (R/W)
DISM2PF	\$D002 (R/W)
DISM3PF	\$D003 (R/W)
DISP0PF	\$D004 (R/W)
DISP1PF	\$D005 (R/W)
DISP2PF	\$D006 (R/W)
DISP3PF	\$D007 (R/W)
DISM0P	\$D008 (R/W)
DISM1P	\$D009 (R/W)
DISM2P	\$D00A (R/W)
DISM3P	\$D00B (R/W)
DISPOP	\$D00C (R/W)
DISP1P	\$D00D (R/W)
DISP2P	\$D00E (R/W)
DISP3P	\$D00F (R/W)

These registers disable (when the corresponding bit is set) independently each collision, respectively to the collision registers. Only 4 lower bits of each register are used. Default value of each register is 00h. These flags can only be accessed when the SPECEN flag is set. Write to HITCLR when SPECEN flag is set, resets all these registers.

KOLM0P \$D008 (R)

Bit	7	6	5	4	3	2	1	0
	SDA	0	0	0	COLPM3	COLPM2	COLPM1	COLPM0

Bit 7 – SDA

This flag provides the status of the SDA line of the TPI I²C interface. This flag can only be accessed when the TPI flag is set. The TPI is the Silicon Image HDMI Transmitter Programming Interface. Description of the TPI interface is contained in the “TPI Programmer’s Reference” (Sil-PR-1032) document. The programmer should remember that the TPI interface is used also by the internal AVR microcontroller and shouldn’t use the interface for about 100 ms after changing the RES2:0 or HDMI flag.

SIZEP0 \$D008 (W)

Bit	7	6	5	4	3	2	1	0
	SDA	SCL	-	-	-	-	SIZEP0	

Bit 7:6 – SDA:SCL

These flags control TPI I²C interface. These flags can only be accessed when the TPI flag is set.

REV \$D015 (R)

Bit	7	6	5	4	3	2	1	0
	1	REV						

This register provides the revision ID of the SOPHIA's core. Bit 7 (always 1) determines the Sophia 3 presence. This register can only be accessed when the SPECEN flag is set.

PRIOR \$D01B

Bit	7	6	5	4	3	2	1	0	Dir
SPECEN:0	GTIAMOD1	GTIAMOD0	MCPLAY	FIFTHPL	PRIOR3	PRIOR2	PRIOR1	PRIOR0	W
SPECEN:1	VGA	RES2	RES1	RES0	PALE3	PALE2	PALE1	PALE0	R/W
Initial	-	-	-	-	0	0	0	0	

Bit 7 – VGA

This flag sets the analog RGB video output to the VGA standard with H:31kHz; V:60/50Hz. The video mode is 480p/576p. This flag can only be accessed when the SPECEN flag is set.

Bits 6:4 – RES2:0 Resolution of the DVI video

These flags sets the DVI output resolution as follows:

RES2	RES1	RES0	Resolution	Aspect Ratio
0	0	0	480p/576p	3:2/5:4
0	0	1	1280x960	4:3
0	1	0	1280x1024	5:4
0	1	1	1344x960	14:10
1	0	0	1440x900	16:10
1	0	1	1536x960	16:10
1	1	0	1600x900	16:9
1	1	1	1704x960	≈16:9

These flags can only be accessed when the SPECEN flag is set.

Bits 3:0 – PALE3:0 Color Palette

These flags choose one of 16 active color palette. Palette #0 is default, standard PAL or NTSC palette. Palettes #1...15 are user programmable in the embedded RAM. These flags can only be accessed when the SPECEN flag is set. The composite and TV, PAL/NTSC encoded outputs uses always only default palette.

FIELD \$D01C

Bit	7	6	5	4	3	2	1	0	Dir
SPECEN:0	FIELD	0	0	0	1	1	1	1	R

Bit 7 – FIELD

This flag provides the parity of the current field of the image. Active only when **INTERLACE** flag is set otherwise is always 0.

VDELAY \$D01C

Bit	7	6	5	4	3	2	1	0	Dir
SPECEN:0	VDELAY7	VDELAY6	VDELAY5	VDELAY4	VDELAY3	VDELAY2	VDELAY1	VDELAY0	W
SPECEN:1	AUDIO	TPI	GR10SHD	CSYNCTL	-	-	-	-	R/W

Bit 7 – AUDIO

This flag controls the digital output mode. When set, the DVI_with_AUDIO mode is selected, otherwise the pure DVI mode. This flag can only be accessed when the SPECEN flag is set.

Bit 6 – TPI

This flag, if set, enables TPI I²C interface. This flag can only be accessed when the SPECEN flag is set.

Bit 5 – GR10SHD: GR.10 Shift Disable

This flag, if set, disables the one-color-cycle shift of the Graphics 10 pixels. This flag can only be accessed when the SPECEN flag is set.

Bit 4 – CSYNCTL: CSYNC Control

This flag controls the level of CSYNC pulses as follows:

CSYNCTL	CSYNC level
0	0.3Vpp@75ohm
1	TTL

This flag can only be accessed when the SPECEN flag is set.

GRACTL \$D01D

Bit	7	6	5	4	3	2	1	0	Dir
SPECEN:0	SPECEN	-	-	-	-	TRIGLEN	PLAYEN	MISSEN	W
SPECEN:1		SYNCTL	VGATE	HIRESBC	LUMOEN	INTERLACE	YUVRGB	NVEN	R/W
Initial	0	-	-	-	-	-	-	-	

Bit 7 – SPECEN: Special Features Enable

This flag, if set, enables an access to the SOPHIA special features flags. This flag, when clear, also resets the Palette RAM address counter.

Bit 6 – SYNCTL: SYNC Control

This flag controls the analog sync outputs as follows:

Mode	SYNCTL	H Output	V Output
RGB	0	CSYNC	RGB Blanking
	1	HSYNC TTL	VSYNC TTL
VGA	X	HSYNC TTL	VSYNC TTL

This flag can only be accessed when the SPECEN flag is set.

Bit 5 – VGATE: Visible Playfield Gate

This flag, if set, limits the playfield width to 168 color cycles (336 high resolution pixels). This flag can only be accessed when the SPECEN flag is set.

Bit 4 – HIRESB: Hi-Res Bi-Color

This flag, if set, enables bi-color high resolution graphics. The color of the graphics pixels is determined by the COLPF1 register, while the color of the playfield is determined by the COLPF2 register. This flag can only be accessed when the SPECEN flag is set.

Bit 3 – LUMOEN: LUM0 bit Enable.

This flag, if set, enables 16 levels of luminance for all graphics modes. This flag can only be accessed when the SPECEN flag is set.

Bit 2 – INTERLACE

This flag controls the analog synchronization mode. When set, the interlaced mode is selected, otherwise the progressive mode. This flag can only be accessed when the SPECEN flag is set.

Bit 1 – YUVRGB

This flag controls the analog color space. When set, the RGB space is selected, otherwise the YP_BP_R space. This flag can only be accessed when the SPECEN flag is set.

Bit 0 – NVEN: Nov-Volatile Memory Enable

This flag enables for a short time an access to the nonvolatile memory. Next write to the GRACTL or PRIOR register will activate transfer of the current values of the red marked flags to the nonvolatile memory. Write operation must be executed within next 4 machine cycles after NVEN flag is set. This feature protects nonvolatile memory against a undesirable write operations. This flag can only be accessed when the SPECEN flag is set.

SOPHIA \$D01E (R)

Bit	7	6	5	4	3	2	1	0
	SOPHIA							
Initial	0	1	0	1	0	0	1	1

This register indicates the SOPHIA 2/3 device presence. The constant value is 53 hex ("S"). This register can only be accessed when the SPECEN flag is set.

PALDATA \$D01F (W)

This register is the Palette RAM data register. Each palette takes 768 bytes RAM. Each color is programmed in three consecutive bytes, as follows:

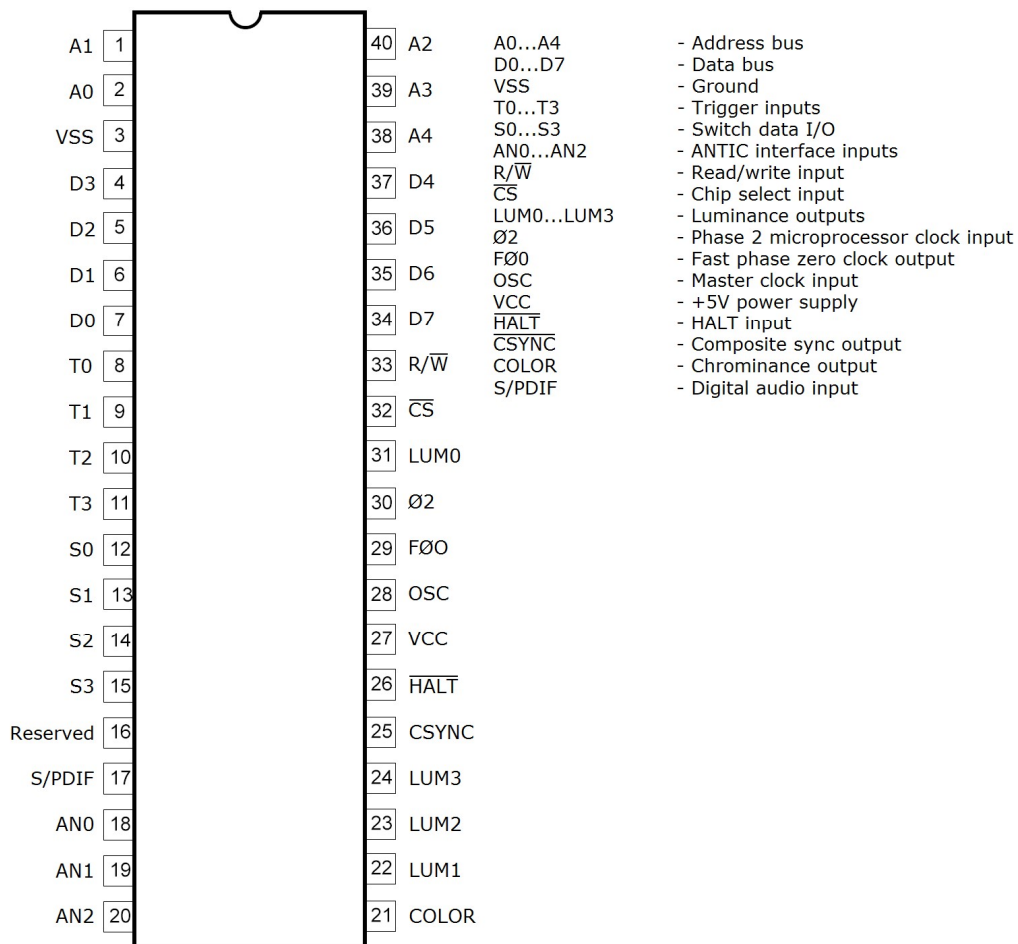
Bit	7	6	5	4	3	2	1	0
Lo	R5	R4	R3	R2	R1	R0	x	x
Me	G5	G4	G3	G2	G1	G0	x	x
Hi	B5	B4	B3	B2	B1	B0	x	x

Each write cycle increments the address counter, therefore programming all 15 palettes requires 11520 write cycles. Address counter has a capacity of 12288 bytes. The last 768 bytes are unused. This register can only be accessed when the SPECEN flag is set. The SPECEN flag, when clear, also resets the address counter.

5. EEPROM Locations

Bit	7	6	5	4	3	2	1	0
00h	x	x	nAUDIO	nTPI	nGR10SH	nCSYNCTL	nVGA	nRES2
01h	nRES1	nRES0	nSYNCTL	nVGATE	nHIRESB	nLUMOE	nINTERL	nYUVRGB

6. Pinout



7. S/PDIF Input Specification

Voltage level: $0.8V \pm 0.2V_{pp}$

Input impedance: 75 ohm

DC offset voltage: $\pm 2V$ max

Audio handling mode: Pass All Audio Modes